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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 March 2003 (20.03.2003)

PCT

(10) International Publication Number
WO 03/023849 A1

(51) International Patent Classification[7]: H01L 23/02, 21/302, 21/461

(21) International Application Number: PCT/US02/27822

(22) International Filing Date: 29 August 2002 (29.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/952,626 13 September 2001 (13.09.2001) US

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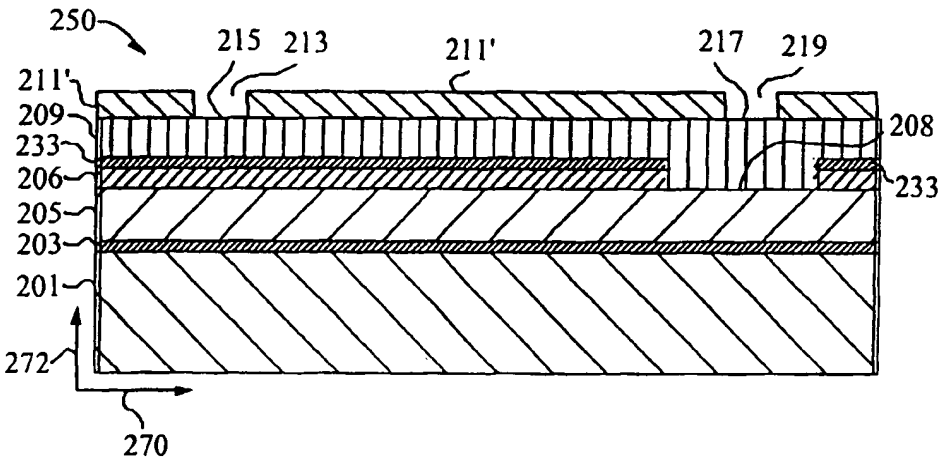
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MICROELECTRONIC MECHANICAL SYSTEM AND METHODS



(57) Abstract: The current invention provides for encapsulated release structures, intermediates thereof and methods for their fabrication. The multi-layer structure has a capping layer (211) that preferably comprises silicon oxide and/or silicon nitride and which is formed over an etch resistant substrate (203). A patterned device layer (206), preferably comprising silicon nitride, is embedded in a sacrificial material (205, 209), preferably comprising polysilicon, and is disposed between the etch resistant substrate (203) and the capping layer (211). Access trenches or holes (219) are formed into the capping layer (211) and the sacrificial material (205, 209) is selectively etched through the access trenches (219) such that portions of the device layer (206) are released from the sacrificial material (205, 209). The etchant preferably comprises a noble gas fluoride N_gF_{2x} (wherein Ng = Xe, Kr or Ar: and where x = 1, 2 or 3). After etching that sacrificial material (205, 209), the access trenches (219) are sealed to encapsulate (241) released portions the device layer (206) between the etch resistant substrate (203) and the capping layer (211). The current invention is particularly useful for fabricating MEMs devices, multiple cavity devices and devices with multiple release features.

WO 03/023849 A1

Microelectronic Mechanical System and Methods

Field of the Invention:

The present invention relates to wafer processing. More particularly, the present invention relates to methods for encapsulation of microelectronic mechanical systems.

Background of Invention:

The combination microelectronic mechanical systems (MEMS) and integrated circuits (ICs) allows for the possibility to make any number of micro-sensors, transducers and actuators. Unfortunately, typical methods for making MEMS are incompatible methods used to fabricate ICs. Hence, MEMS and ICs are usually fabricated separately and laboriously combined in subsequent and separate steps.

In addition to the MEMS and ICs processing incompatibilities, MEMS typically require encapsulation, whereby the active portions of the MEMS are sealed within a controlled storage environment. One way to encapsulate the active portions of the MEMS is to provide unique customized packaging structure configured with conductive leads fitted for the MEMS. Alternatively, the MEMS can be formed on a wafer substrate that serves as a bottom portion of the packaging structure. After the MEMS is formed on the wafer, then a matched lid structure is glued or soldered over the active potions of the MEMS within the suitable storage environment. For example, Shook describes a method and apparatus for hermetically passivating a MEMS on a semi-conductor substrate in U.S. Patent Application Serial No. 09/124,710, and also U.S. Patent Application Serial No. 08/744,372, filed 7/29/98 and entitled METHOD OF AND APPARATUS FOR SEALING A HERMETIC LID TO A SEMICONDUCTOR DIE, the contents of both of which are hereby incorporated reference.

What is needed is a method to make MEMS and other structures on a wafer substrates utilizing processes that are compatible with standard IC wafer processing, whereby MEMS and ICs are capable of being fabricated on the same wafer chip. Further, what is needed is a method to fabricate MEMS, wherein the active portions of the MEMS are readily encapsulated within a variety of suitable storage environments.

Summary of the Invention:

The current invention provides a method of making an encapsulated release structure. Preferably, the release structure is a MEMS device having a plurality of ribbons or beams,

which may further have a comb structure. In an embodiment of the instant invention, the device comprises a resonator that can be used for periodic waveform generation (e.g. clock generation). In other embodiments, the device comprises a grating light valve for generation and/or transmission of optical information. In yet other embodiments the device comprises a radio frequency (RF) generator for wireless transmission of information.

The release structure is formed between layers of a multi-layer structure. The multi-layer structure preferably comprises a first and second etch-stop layers, which can be the same as or different from each other, and a first sacrificial layer between the first and the second etch-stop layer. Release features are patterned into the second etch-stop layer. Preferably, the multi-layer structure is formed on a silicon wafer substrate. The silicon wafer substrate is preferably configured to couple the MEMS device with an integrated circuit (IC), also formed on the silicon wafer substrate.

Preferably, the multi-layer structure is formed with a first etch-stop layer that is deposited on or over a selected region of the silicon wafer substrate. The first etch-stop layer is preferably a silicon dioxide layer, a silicon nitride layer or a combination thereof. On top of or over the first etch-stop layer the first sacrificial layer is formed. The first sacrificial layer preferably comprises a polysilicon material though other materials can also be used. The second etch-stop layer is formed on or over the first sacrificial layer with a pattern corresponding to release features of the release structure.

The second etch-stop layer is patterned with the release structure features using any suitable patterning technique. Accordingly, a patterned photo-resist is formed on or over the second etch-stop layer prior to removing a portion thereof to form a patterned second etch-stop layer having gaps therein and between portions of the second etch-stop layer under the patterned phot resist. Alternatively, the first sacrificial layer can be anisotropically etched with a positive impression of the release structure features. The positive impression of the release structure features provides nuclei for rapid anisotropic growth of release structure features onto the patterned portions of the first sacrificial layer during the deposition of the second etch-stop layer. Regardless, of the method used to form the second etch-stop layer, a second sacrificial layer is formed over the second etch-stop layer sandwiching the second etch-stop layer having the release structure features between the first and the second sacrificial layers. The second sacrificial layer preferably comprises polysilicon. On top of the second sacrificial layer a sealant layer or capping layer is formed. The capping layer preferably comprises one or more conventional passivation layers and more preferably

comprises a silicon oxide layer, a silicon nitride layer or a combination thereof.

The etch-stop layers are formed by any number of methods. An etch-stop layer can be formed from any materials that show resistance to etching under specified etching conditions relative to the materials that form the sacrificial layer(s). In the instant invention the etching rate (mass or thickness of material etched per unit time) of sacrificial materials(s) relative to the etch-stop layer materials is preferably greater than 10:1, more preferably greater than 50:1 and most preferably greater than 100:1. In developing the present invention, experimental results of approximately 2500:1 have been achieved. Any particular etch-stop layer can comprise one or more layers, any of which can be exposed to the sacrificial layer etchant as long as the etch-stop layer exhibits sufficient resistance to the sacrificial layer etchant.

In an embodiment of the instant invention, one or more of the etch-stop layers of the multi-layer structure comprise silicon oxide. Preferably the silicon oxide is silicon dioxide; when silicon oxide is referred to in this document, silicon dioxide is the most preferred embodiment, although conventional, doped and/or non-stoichiometric silicon oxides are also contemplated. Silicon oxide layers can be formed by thermal growth, whereby heating a silicon surface in the presence of an oxygen source forms the silicon oxide layer. Alternatively, the silicon oxide layers can be formed by chemical vapor deposition processes, whereby an organic silicon vapor source is decomposed in the presence of oxygen. Likewise, the silicon nitride layers can be formed by thermal growth or chemical deposition processes. The polysilicon sacrificial layers are preferably formed by standard IC processing methods, such as chemical vapor deposition, sputtering or plasma enhanced chemical vapor deposition (PECVD). At any time before the formation of a subsequent layer, the deposition surface can be cleaned or treated. After the step of patterning the release structure, for example, the deposition surface can be treated or cleaned with a solvent such as N-methyl-2-pyrolipone (NMP) in order to remove residual photo-resist polymer. Further, at any time before the formation of a subsequent layer, the deposition surface can be mechanically planarized.

After the multi-layer structure is formed with the release structure (e.g. patterned from the second etch-stop) sandwiched between the first and the second sacrificial layers, access holes or trenches are formed in the capping or sealant layer, thereby exposing regions of the second sacrificial layer therebelow. Access trenches are referred to, herein, generally as cavitations formed in the capping or sealant layer which is allows the etchant to etch the material in the sacrificial layer therebelow. For simplicity, the term access trenches is used

herein to encompass both elongated and symmetrical (e.g. holes, rectangles, squares, ovals, etc.) cavitations in the capping or sealant layer.

In accordance with the instant invention, access trenches can have any number of shapes or geometries, but are preferably anisotropically etched to have steep wall profiles. The access trenches are preferably formed by etching techniques including wet etching processes and reactive ion etching processes though other conventional techniques can be used. The exposed regions of the second sacrificial layer are then treated to a suitable etchant which selectively etches substantial portions of the first and second sacrificial layers portion so the release structures are suspended under the capping or sealant layer.

The preferred etchant comprises a noble gas fluoride, such as xenon difluoride. Preferably, the exposed regions of the second sacrificial layer can be treated with a pre-etch solution of ethylene glycol and ammonium fluoride prior to selectively etching the first and second sacrificial layers. The pre-etch solution can prevent the formation of oxide, clean exposed regions of the second sacrificial layer, remove polymers and/or help to ensure that etching is not quenched by the formation of oxides. The etching step is preferably performed in a chamber, wherein the etchant is a gas. However, suitable liquid etchants are considered to be within the scope of the current invention, whereby the noble gas fluoride is a liquid or is dissolved in suitable solvent.

In the preferred method of the instant invention the multi-layer structure is placed under vacuum with a pressure of approximately 10^{-5} Torr. A container with Xenon Difluoride crystals is coupled to the chamber through a pressure controller (e.g. a controllable valve). The crystals are preferably at room temperature within the container with the pressure of Xenon Difluoride of approximately 4.0 Torr. The pressure controller is adjusted such that the pressure within the chamber is raised to approximately 50 milliTorr. This pressure, or an alternatively sufficient pressure, is provided to ensure a controllable etching rate, a positive flow of Xenon Difluoride to the chamber and excellent uniformity of the etch processes.

After the etching step, the access trenches maybe sealed to encapsulate the suspended release structure between the first etch-stop layer and the capping or sealant layer. The sealing step is performed at a separate processing station within a multi-station wafer processing system or, alternatively, is performed within the chamber apparatus. The access trenches can be sealed by any number of methods including sputtering, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or spin on glass

methods. The access trenches can be sealed with any number of materials including metals, polymers and ceramics. Preferably, the access trenches are sealed by sputtering a layer of aluminum over the access trenches and the capping layer. For optical applications, excess aluminum can be removed from the capping or sealant layer using a suitable mechanical or chemical method.

In accordance with alternative embodiments of the invention, before depositing the second sacrificial layer on the patterned second etch-stop layer, the second etch-stop layer may have a reflective material deposited thereon. The reflective material preferably comprises aluminum. Accordingly, after the sacrificial layers are etched away, the release features preferably have a reflective upper surface suitable for optical applications.

In yet other embodiments of the invention, a gettering material, such as titanium or a titanium-based alloy can be deposited within a cavity capped by the capping or sealant layer prior to sealing the access trenches in the capping or sealant layer. The gettering material is provided to help reduce residual moisture and/or oxygen which can lead to performance degradation of the device over time. The release structure is preferably sealed under a vacuum or, alternatively, under a suitable noble gas atmosphere, as described in detail below.

The invention provides a sealed MEMS device on an IC chip, intermediate elements thereof and also a method of forming the same using techniques that are preferably compatible with standard IC processing. For example, the method of the instant invention provides for processing steps that are preferably carried out at temperatures below 600 degrees Celsius and more preferably at temperatures below 550 degrees Celsius. Further, the current invention provides for a method to fabricate MEMS with active structures which are hermetically sealed in a variety of environments. The current invention is not limited to making MEMS and can be used to make any number of simple or complex multi-cavity structures that have micro-fluid applications or any other application where an internalized multi-cavity silicon-based structure is preferred. Also, as will be clear for the ensuing discussion that the method of the instant invention is capable of being used to form any number of separate or coupled release structures within a single etching process and that larger devices can be formed using the methods of the instant invention.

Brief Description of the Drawing:

Figure 1 is a schematic illustrating a MEMS oscillator.

Figures 2a-h illustrate top views and cross-sectional views a multi-layer structure

formed on silicon wafer substrate, in accordance with current invention.

Figures 3a-f show cross sectional views of a release features being formed from a multi-layer structure, in accordance with a preferred method of the current invention.

Figure 4 is a block diagram outlining steps for forming a multi-layer structure illustrated in Figure 3a.

Figure 5 is a block-diagram outlining the method of forming a release structure from the multi-layered structure shown in Figure 2a.

Figure 6 is a block-diagram outlining the steps for etching sacrificial layers of the multi-layer structure illustrated in Figure 2b.

Figure 7 is a schematic diagram of a chamber apparatus configured to etch a multi-layered structure formed in accordance with the method of instant invention.

Detailed Description of the Invention:

In general, the present invention provides a method to make devices with encapsulated release structures. The current invention is particularly useful for fabricating MEMS oscillators, optical display devices, optical transmission devices, RF devices and related devices. MEMS oscillators can have any number or simple or complex configurations, but they all operate on the basic principle of using the fundamental oscillation frequency of the structure to provide a timing signal to a coupled circuit. Referring to Figure 1, a resonator structure 102 has a set of movable comb features 101 and 101' that vibrate between a set of matched transducer combs 105 and 105'. The resonator structure 102, like a pendulum, has a fundamental resonance frequency. The comb features 101 and 101' are secured to a ground plate 109 through anchor features 103 and 103'. In operation, a dc-bias is applied between the resonator 102 and a ground plate 109. An ac-excitation frequency is applied to the comb transducers 105 and 105' causing the movable comb features 101 and 101' to vibrate and generate a motional output current. The motional output current is amplified by the current to-voltage amplifier 107 and fed back to the resonator structure 102. This positive feed-back loop destabilizes the oscillator 100 and leads to sustained oscillations of the resonator structure 102. A second motional output current is generated to the connection 108, which is coupled to a circuit for receiving a timing signal generated by the oscillator 100.

Referring now to Figure 2a showing a plan view of a wafer, a wafer structure 200 preferably comprises a silicon substrate 201 and a first etch-stop layer 203. The first etch-

stop layer 203 may not be required to perform the methods of the instant invention, especially when the silicon substrate 201 is sufficiently thick to allow sacrificial layers to be etched without completely etching away the silicon substrate 201. Also, the substrate 201 itself can be formed from or doped with a material that renders the substrate 201 substantially resistant to the etchant that is used, such that the formation of the first-etch-stop layer 203 is not required. However, in an alternative embodiment, a material that can be selectively etched relative to a silicon substrate can be selected or used as the sacrificial layer. The first etch-stop layer 203 preferably comprises silicon oxide, silicon nitride, a combination thereof or any other suitable material which exhibits sufficient resistance to the etchant used to etch the first sacrificial layer.

Still referring to Figure 2a, a region 251 of the wafer structure 200 is used to form the release structure. Other portions of the wafer structure 200 can be reserved for forming an integrated circuit that can be electrically coupled to and that can control operation of the release structure formed in the region 251. In addition, any number of release structures and release structure region 251 can be formed on the same wafer structure 200.

Now referring to Figure 2b, in the region 251, a first sacrificial layer 205 is formed over the first etch-stop layer 203 using any conventional technique. The first sacrificial layer 205 is formed from any suitable material that is selectively etched relative to the underlying first etch-stop layer(s), but preferably comprises polysilicon.

Referring now to Figure 2c, a second etch-stop layer 207 is formed over the first sacrificial layer 205. The second etch-stop layer 207 can be formed of the same or different material as the first etch-stop layer 203. The second etch-stop layer 207 preferably comprises silicon oxide, a silicon nitride, a combination thereof or any other suitable material which exhibits sufficient resistance to the etchant used. In an embodiment of the invention, the first sacrificial layer 205 is etched prior to depositing the second etch-stop layer 207 to provide raised support features 215 and 215' which support the subsequently formed release structures. Alternatively, or in addition to forming the raised support features 215 and 215', support posts may be formed 216, 216' and 216" in positions to provide support for the release structures formed in subsequent steps. Preferably, the support posts 216, 216' and 216" are formed from an etch resistant material(s) that are the same or different than material(s) used to form the etch-stop layer 203 and/or etch-stop layer 207 and capping layer 211, as described in detail below.

Alternatively to forming support features 215 and 215' and/or support posts 216, 216'

and 216", or in addition to forming the support features 215 and 215' and/or support posts 216, 216' and 216", the second etch-stop layer 207 can be deposited in an area of the region 251 without underlying sacrificial layer 205 and such portions of the second etch-stop layer 207 maybe deposited directly onto and/or attached to the first etch-stop layer 203 and/or substrate 201, such as shown in Figure 2 d. After the second etch-stop layer 207 is patterned and the sacrificial layer 205 is etched, portions of the second etch-stop layer 207 deposited directly on the first etch-stop layer 203 provide structural supports for the release structures formed. There are any number of mechanisms to provide physical support for the release structures formed that are considered to be within the scope of the instant invention.

Now referring to Figure 2e, in accordance with a preferred embodiment of the instant invention a reflective layer 233 is deposited over the second etch-stop layer 207 and/or the support features 215 and 215' and/or support posts 216, 216' and 216". The reflective layer 233 preferably comprises aluminum or other suitable reflective material. The reflective layer 233 is preferably resistant to enchant being used in removing the sacrificial layers, but is capable of being etched using other suitable techniques including photo-lithograph and plasma etch, wherein the patterned release structures formed in subsequent steps have reflective surfaces suitable for optical applications. Preferably, a set of bond pad 226, 227 and 228 are also formed on the wafer structure 200 for electrically coupling the release structure(s) to a circuit external to the integrated circuit containing/comprising the release structure(s). It will be readily understood by those of ordinary skill in the art that the reflective layer 233 can alternatively be deposited on the release features 204 and 206 after they are formed.

Now referring to Figure 2f, the reflective layer 233 and the second etch-stop layer 207 is patterned to form the release structures/features 204 and 206. The reflective layer 233 and the second etch-stop layer 207 are preferably patterned using conventional photo-lithography techniques and/or steps. For example, a photo-resist layer is formed on the reflective layer 233. The photo-resist is patterned and developed to form a patterned phot-resist mask (not shown). Portions of the reflective layer 233 and the second etch-stop layer 207 are then removed using conventional techniques leaving the patterned features 204 and 206 with a reflective layer 233 under the patterned photo-resist mask. The patterned photo-resist mask can then be removed from the patterned features 204 and 206 and the patterned features 204 and 206 can be encapsulated as described in detail below.

Alternatively, the first sacrificial layer 205 can be etched with a positive impression

of the release features (not shown). The positive impression of the release features then provide nuclei for rapid anisotropic growth of release structure features 204 and 206. The release features 204 and 206 are shown in Figure 2f as comb structures. However, it is clear that the release features can be comb structures, ribbon structures, cantilevers or any number of other structures including, but not limited to, domain separators, support structures and/or cavity walls as described in detail below. Further, while providing a reflective layer 233 is preferred, the additional step of forming a reflective layer 233 is not required when the patterned features 204 and 206 are not used to reflect light, such as in the case for micro-fluidic devices. The line 270 shows an x-axis of the wafer structure 200 and the line 271 shows the y-axis of the wafer structure. The z-axis 272 of the wafer structure 272 in Figure 2f is normal to the view shown.

Figure 2g shows a side cross-sectional view of the wafer structure 200 after a second sacrificial layer 209 is deposited over release features 204 and 206 with the reflective layer 233. In the Figure 2g, the y-axis 271 is now normal to the view shown and the z-axis 272 in now in the plane of the view shown. The release features 204 and 206 are embedded between the sacrificial layers 205 and 209 and the sacrificial layers 205 and 209 are preferably in contact through gap regions between the release features 204 and 206. The second sacrificial layer 209 is formed of any suitable material that is selectively etched relative to the etch-stop layer(s) used to form the release structure device, but preferably comprises polysilicon.

Now referring to Figure 2h, after the second sacrificial layer 209 is deposited over the release features 204 and 206, a capping layer 211 is deposited over the second sacrificial layer 209. The capping layer 211 preferably comprises silicon dioxide, silicon nitride any combination thereof or any other suitable material(s) which exhibit(s) sufficient resistance to the etchant used. The capping layer 211 can be formed of the same or different material as the first etch-stop layer 203 and/or the second etch-stop layer 207. Figures 3a-3f will now be used to illustrate the preferred method of forming an encapsulated release structure from a portion 250 of the structure 200 as shown in Figure 2h.

Referring now to Figure 3a, a device with a release structure, such as the MEMS resonators structure 102 described above, is preferably made from a multi-layer structure 250. The multi-layer structure 250 has a first etch-stop layer 203 that is preferably formed on the region 251 of the silicon wafer substrate 201, such as previously described. The first etch-stop layer 203 may comprise any material or materials that exhibit resistance to etching

under the conditions for etching the first sacrificial layer. For example, when the first etch sacrificial layer comprises polysilicon, the first sacrificial layer etchant comprises XeF_2, and the first sacrificial layer etching conditions are described below for etching polysilicon with XeF_2. The first etch-stop layer 203 preferably comprises a silicon oxide layer or a silicon nitride layer with a layer thickness in a range of 500 to 5000 Angstroms.

On top of the first etch-stop layer 203 there is formed a first sacrificial layer 205. The first sacrificial layer 205 may comprise any materials(s) that may be selectively etched relative to the underlying first etch-stop layer 203 (when present) or substrate 201 (when the first etch-stop layer is not present). However, when the first etch-stop layer 203 comprises silicon oxide or silicon nitride, the first sacrificial layer 205 preferably comprises a polysilicon. Alternatively, the first sacrificial layer 205 can comprise a doped silicon oxide layer that is doped with boron, phosphorus or any other dopant which renders the first sacrificial layer 205 to be preferentially etched over the substrate 201 or etch-stop layer 203 and/or the etch-stop layer 206 and capping layer 211, described in detail below. The first sacrificial layer 205 preferably has a layer thickness in a range of 0.1 to 3.0 microns.

On top of the first sacrificial layer 205 is formed a second etch-stop layer 207. The second etch-stop layer 207 is patterned with features 206 and 204 corresponding to the release structure. The first etch-stop layer 203 may comprise any material(s) that exhibit resistance to etching under the conditions for etching the first sacrificial layer. For example, when the first sacrificial layer 205 comprises polysilicon, the first sacrificial layer etchant comprises XeF_2, and the first sacrificial layer etching conditions are described below for etching polysilicon with XeF_2. The second etch-stop layer 207 preferably comprises a silicon oxide layer or a silicon nitride layer with a layer thickness in a range of 300 to 5000 Angstroms.

On the second etch-stop layer 207 is formed a second sacrificial layer 209. The second sacrificial layer 209 may comprise any materials(s) that may be selectively etched relative to the underlying, the second etch-stop layer 207 and/or the first etch stop layer 203 (when present) or substrate (when the first etch-stop layer is not present). However, when the first and the second etch-stop layers 203 and 207 comprise silicon oxide or silicon nitride, the second sacrificial 209 layer preferably comprises a polysilicon. Alternatively, second first sacrificial layer 209 can comprise a doped silicon oxide layer that is doped with boron, phosphorus or any other dopant which renders the sacrificial layer 209 to be preferentially etched over the substrate 201 or etch-stop layers 203 and 207. The second sacrificial layer

209 preferably has a layer thickness in a range of 0.1 to 3.0 microns and preferably, the sacrificial layers 205 and 209 are in contact with each other in the patterned regions 208 or gaps between the features 206 and 204 of the release structure.

A capping or sealant layer 211 is deposited over second sacrificial layer 209. The capping or sealant layer 211 preferably comprises a conventional passivation material (e.g. an oxide, nitride, and/or an oxynitride of silicon, aluminum and/or titanium). The capping or sealant layer 211 also can comprise a silicon or aluminum-based passivation layer which is doped with a conventional dopant such as boron and/or phosphorus. More preferably, the capping layer or sealant layer 211 comprises a silicon oxide layer with a layer thickness in a range of 1.0 to 3.0 microns. It will be apparent to one of ordinary skill in the art that though the layers referred to above are preferably recited as being single layer structures, each can be formed of a sandwich of known layers to achieve the same result. Furthermore, though the layers are preferably taught as being formed one on top of the next, it will be apparent that intervening layers of varying thicknesses can be inserted.

Now referring to Figure 3b, access trenches 213 and 219 are formed in the capping layer 211 thereby exposing regions 215 and 217 of the second sacrificial layer 209. The access trenches 213 and 219 are preferably anisotropically etched, although the access trenches 213 and 219 may be formed by any number of methods including wet and/or dry etching processes. For example, a photo-resist is provided on the capping layer and is exposed and developed to provide a pattern for anisotropically etching the access trenches 213 and 219. Alternatively, an etchant may be selectively applied to a portion of the etch-stop layer 211 corresponding to the access trenches 213 and 219. For example micro-droplets or thin streams of a suitable etchant can be controllably applied to the surface of the capping or sealant layer 211 using a micro-syringe technique, such as described by Dongsung Hong, in U.S. Patent Application No. 60/141,444, filed June 29, 1999 (Attorney Docket No. 0325,00226), the contents of which are hereby incorporated by reference.

After the access trenches 213 and 219 are formed in the capping layer 211, when the second sacrificial layer comprises polysilicon, the exposed regions 215 and 217 of the second sacrificial layer 209 can be treated with a pre-etch solution of ethylene glycol and ammonium fluoride. A suitable pre-mixed solution of ethylene glycol and ammonium fluoride is commercially available under the name of NOE Etch I ™ manufactured by ACSI, Inc., Milpitas, CA 95035. Oxides can form on the surfaces of exposed polysilicon regions, such as 215 and 217. Such oxides can interfere with polysilicon etching and result in an incomplete

etch. The pre-etch solution is believed to prevent and/or inhibit the formation of oxides on the surfaces of the exposed regions 215 and 217, or removes such oxides if present and/or formed, to avoid incomplete etching of the sacrificial layers 205 and 209.

Now referring to Figure 3c, after the access trenches 213 and 219 are formed in the capping layer 211, the sacrificial layers 205 and 209 are selectively etched to release the features 204 and 206. The features 204 and 206 can have any number of different geometries. For example, in the fabrication of a MEMS device the release features are comb or ribbon structures. In the fabrication of a micro-fluidic device the release features provide pathways which interconnect cavities 221 and 223. In the fabrication of electronic levels or electronic accelerometers the release features can be cantilevers. After the features 204 and 206 are released, then the access trenches 213 and 219 in the layer 211' are sealed to encapsulate the features 204 and 206 between the layers 203 and 211'.

Now referring to Figure 3d, in further embodiments of the instant invention, prior to sealing the access trenches 213 and 219 in the layer 211', a gettering material 231 such as titanium or a titanium-based alloy can be deposited within at least one of structure cavities 221 and 223 through the access trenches 213 and 219. Alternatively, gettering material/agent 231 can be deposited at the time that the reflective layer 233 is formed. In yet further embodiments, a gettering material 231 is a dopant within the sacrificial layer 205 and 209 that is released during the etching of the sacrificial layers 205 and 209.

Now referring to Figure 3e, after surfaces of the cavities 221 and 223 and/or the features 204 and 206 are treated and provided with a suitable environment, as described in detail below, the access trenches 213 and 219 are preferably sealed. The release features 204 and 206 are preferably sealed under a vacuum, but can be sealed within a predetermined or controlled gas and/or liquid for some applications. The access trenches 213 and 219 are sealed by any of a number of methods and using any of a number of materials including metals, polymers and/or resins. Preferably, the access trenches 213 and 219 are sealed by sputtering conventionally sputtered metals over the access trenches 213 and 219 and the capping layer 211 and more preferably by sputtering aluminum over the access trenches 213 and 219 and capping layer to form the layer 242.

Now referring to Figure 3f, for optical applications, a portion of the layer 242 can be removed such that corking structures 240 and 241 remain in the access trenches 213 and 219. The capping layer 211 may provide an optical window through which light can pass to the layer 233 on the release features 204 and 206. Portions of the layer 242 are preferably

removed by micro-polishing techniques. Alternatively, conventional photo-lithography techniques can be used to etch away a portion of layer 242.

In an embodiment of the invention, portion of the layer 242 of the layer is selectively removed such that the capping layer 211 provides an optical aperture (not shown) through which light can pass to and/or from the layer 233 on the release features 204 and 206.

Figure 4 is a block diagram flow chart 300 outlining steps for forming a multi-layer structure shown in Figure 3a in accordance with a preferred method of the instant invention. The multi-layer structure shown in Figure 3a is preferably made by sequential deposition processes, such as described above, wherein the uniformity and thicknesses of each of the structure layers are readily controlled.

Still referring to Figure 4, in the step 301, a silicon dioxide layer is formed by steam or dry thermal growth on a silicon substrate or by deposition on a selected region of the silicon wafer or other substrate. Preferably, the silicon dioxide layer is thermally grown to a thickness in a range of 250 to 5000 Angstroms and more preferably in a range of 250 to 750 Angstroms. The thermal oxidation occurs by placing the wafer substrate at a temperature in a range of 600 to 800 degrees Celsius in a controlled oxygen environment. In the step 303, a polysilicon layer is preferably deposited by Low Pressure Chemical Vapor Deposition (LPCVD) on the first etch stop layer to a thickness in a range of 0.1 to 3.0 microns and more preferably to a thickness in a range of 0.5 to 1.0 microns. Low Pressure Chemical Vapor Deposition of the amorphous polysilicon is preferably carried out at temperatures in a range of 450 to 550 degrees Celcius.

After the first polysilicon layer is deposited in the step 303, then in the step 305 a silicon nitride device layer is formed on the first poly silicon sacrificial layer. Preferably, the silicon nitride layer is formed by LPCVD to a thicknesses in a range of 300 to 5000 Angstroms and more preferably in a range of 750 to 1250 Angstroms. The silicon nitride device layer can be formed by thermal decomposition of dichlorosilane in the presence of ammonia.

In accordance with alternative embodiment of the current invention, the silicon nitride layer is patterned with structure features after the deposition of a photo-resist layer is deposited, exposed and developed (thereby forming an etch mask) in the step 303, or by selectively etching a pattern into the first polysilicon layer formed in the step 303 to initiate rapid growth of the silicon nitride in the etched areas of the polysilicon layer. Preferably, the silicon nitride layer is deposited as a continuous layer which is then selectively etched to

form the release features of the release structure using a conventional photo-resist mask.

After forming the patterned silicon nitride layer in the step 305, then in the step 307 a second sacrificial layer is formed over the patterned silicon nitride layer, sandwiching the patterned layer between the first and the second sacrificial layers. The second sacrificial layer is preferably also a polysilicon layer that is preferably deposited by LPCVD to a thickness in a range of 0.1 to 3.0 microns and more preferably to a thickness in a range of 0.5 to 1.0 microns. The second sacrificial layer is preferably formed by thermal decomposition of an organosilicon reagent, as previously described. Preferably, the first and the second polysilicon layer have contact points whereby the etchant can pass through the contact points between the first and the second sacrificial layers to etch away portions of both the first and the second polysilicon sacrificial layers. Preferably, in the step 311, and prior to the step 305 of forming the second polysilicon layer, the deposition surface of the patterned silicon nitride layer is treated with a solvent such NMP (which can be heated) to clean its surface. In accordance with the method of the current invention, surfaces can be treated at any time during the formation of the multi-layer structure to remove residues thereon that may lead to poor quality films.

After the second polysilicon layer is formed in the step 307, then in the step 309, a capping layer is formed over the second polysilicon layer. The capping layer is preferably a silicon oxide capping layer deposited by Plasma Enhanced Chemical Vapor deposition (PECVD) to a thickness in a range or 1.0 to 3.0 microns and more preferably in a range of 1.5 to 2.0 microns. In the PECVD process, an organosilicon compound, such as a tetraethyl orthosilicate (TEOS), is decomposed in the presence of an oxygen source, such as molecular oxygen, to form the silicon oxide capping layer. In the step 310, and prior to the step 309, the second polysilicon layer may be planarized and/or cleaned to prepare a suitable deposition surface for depositing or forming the capping layer.

Figure 5 is a block diagram flow chart 400 outlining the preferred method of forming a device from the multi-layered structure shown in Figure 3a. In the step 401, access trenches are formed in the capping layer. The access trenches are formed with diameters in a range of 0.4 to 1.5 microns and more preferably in a range of 0.6 to 0.8 microns. The access trenches are preferably formed in the silicon oxide capping layer using a reactive ion etch process. The reactive ion etch process can, under known or empirically determined conditions, etch trenches with sloped or straight walls which can be sealed in a subsequent step or steps. The access trenches are preferably formed through the capping layer to

exposed regions of the sacrificial material therebelow. Preferably, in step 402, and prior to the step 403, the exposed regions of the sacrificial layer are treated with a pre-etch cleaning solution of ethylene glycol and ammonium fluoride, that comprises approximately a 10% by weight solution of ammonium fluoride dissolved in ethylene glycol. After the exposed regions of the sacrificial layer are treated with the pre-etch solution in the step 402, then in the step 403 the polysilicon layers are selectively etched with an etchant comprising a noble gas fluoride NgF_{2x}, (wherein Ng = Xe, Kr or Ar, and where x = 1, 2 or 3). More preferably, the etchant comprises xenon difluoride. Further advantages of using xenon difluoride etchant are described by Pister in U.S. Patent No. 5,726,480, the contents of which are hereby incorporated by reference.

After the etching step 403 is complete, then in the step 404 a gettering material may be deposited through one or more of the access trenches into the device cavity formed during the etching step 403. In the step 405, the access trenches are sealed by sputtering aluminum onto the capping layer sufficiently to seal the access trenches. Excess aluminum can be removed from the capping layer by well known methods such as chemical, mechanical polishing or phot-lithography.

Figure 6 is a block diagram outlining the preferred method of etching the polysilicon sacrificial layers in the step 403 shown in Figure 5. After the access trenches are formed in the step 401, and the exposed regions of the polysilicon layer are treated in the step 402, as described above, then in the step 501, the structure is place under a vacuum of approximately 10^{-5} torr. In the step 503, xenon difluoride crystals are preferably sublimed at a pressure in a range of 0.1 to 100 Torr, more preferably in a range of 0.5 to 20 Torr and most preferably at approximately 4.0 Torr. In the step 505, a controlled stream of xenon difluoride is provided to the chamber. The chamber is preferably maintained at a pressure lower than the sublimation pressure of the xenon difluoride crystals to ensures a positive flow of the xenon difluoride to the chamber. The pressure in the chamber is preferably maintained in a range of 0.1 milliTorr to 1.0 Torr, more preferably in a range of 1.0 milliTorr to 100 milliTorr and most preferably at approximately 50 milliTorr (0.05 Torr).

Figure 7 illustrates a schematic diagram of an apparatus 600 for carrying out the etching step described in block-flow diagram 500 shown in Figure 5. The apparatus 600 is preferably coupled with a vacuum source 607 that is capable of drawing a vacuum in the chamber environment 605'. The apparatus 600 preferably includes a pressure measuring device 609 that allows a user to monitor the pressure within the chamber 610. A container

608 containing an etchant source (e.g. crystals of xenon difluoride) is coupled to the chamber 610 through a pressure or flow controller 613. The container 608 can have a pressure measuring device 611 coupled to the container 608 to allow the user to monitor the pressure within the container 608.

In operation, a multi-layer structure 620, similar to those described previously, is placed in the chamber 610. The vacuum control valve is opened and the vacuum source 607 draws a vacuum reducing the pressure of the chamber environment 605' preferably to or near to 10^{-5} Torr. Under known conditions, the xenon difluoride crystals at room temperature form a vapor pressure of XeF_2 of approximately 4.0 Torr, as determined by the pressure measuring device 611. The pressure controller 613 is adjusted to change the pressure of the chamber environment 605' to approximately 50 x 10^{-3} Torr. The structure 620 is etched for a time sufficient to form the release structure 623 within the cavity 621 of the structure 620. The etching process takes place over a period of approximately 20-30 minutes, depending on the etching pressure chosen, the physical details of the structure 620 and flow dynamics of the chamber apparatus 600.

After the etching step is complete, a suitable sealing environment may then be provided. Accordingly, in one embodiment the patrial pressure control value 613 is shut off and a low pressure vacuum is reestablished using a draw from the vacuum source 607. The trenches of the etched structure 620 may be sealed by a sputter beam 650 of aluminum, using a sputter device 630.

Alternatively, after reestablishing a low pressure vacuum, the chamber may be backfilled with a noble gas. Accordingly, a noble gas source 615 may be coupled to the control chamber 610 through a control valve 612. The chamber environment 605' is flushed with a noble gas by opening the gas valve 612 prior to sealing the trenches of the device 620. The trenches of the device 620 may then be sealed with a polymer or ceramic material, thereby capturing a portion of the chamber environment 605' within the cavity 621 of the device 620.

The above examples have been described in detail to illustrate the preferred embodiments of the instant invention. It will be clear to one of ordinary skilled in the art that there are many variations to the invention that are within the scope of the invention. For example, a device with multiple layers of release structures can be formed by extending teachings of the invention and using multi-layer structures having more than one pattered layer. Further, it is clear that any number of devices with coupled and un-coupled release

structures and with multi-cavity structures are capable of being fabricated using the method of the instant invention.

CLAIMS

What is claimed is:

1. A method of making a release structure from a multi-layer structure comprising first and second etch-stop layers, a first sacrificial layer between the first and the second etch-stop layers, a cap layer and a second sacrificial layer between the second etch-stop layer and the cap layer with at least one access trench, wherein the second etch-stop layer includes a release feature, the method comprising;
   a. creating an access opening in the cap layer; and
   b. etching portions of the first and the second sacrificial layers through the at least one access opening to form the release structure.

2. The method of claim 1, further comprising the step of applying a pre-etch solution in the at least one access trench prior to the etching step.

3. The method of claim 1, wherein each of the first and second etch-stop layers are formed of a material selected from the group consisting of oxides, oxynitrides and nitrides of silicon.

4. The method of claim 1, wherein the first sacrificial layer and the second sacrificial layer comprise polysilicon.

5. The method of claim 4, wherein the first sacrificial layer and the second sacrificial layer independently have a thickness in a range of 0.1 to 3.0 microns thick.

6. The method of claim 1, wherein the multi-layer structure further comprises a silicon substrate.

7. The method of claim 6, wherein the first sacrificial layer, the second etch-stop layer, the second sacrificial layer and the cap layer are formed by sequential deposition on the silicon substrate.

8. The method of claim 1, wherein the access opening is formed by anisotropically

etching the cap layer.

9. The method of claim 1, wherein the etching portions of the first and second sacrificial layers is performed with an etchant comprising a noble gas fluoride.

10. The method of claim 1, wherein the etching portions of the first and second sacrificial layers is performed with an etchant comprising xenon difluoride.

11. The method of claim 1, further comprising sealing the access opening with a sealing material.

12. The method of claim 11, wherein the sealing material comprises a material selected from the group consisting of polymers, metals and ceramics.

13. The method of claim 11, wherein the sealing material is aluminum metal.

14. The method of claim 1, wherein the release structure comprises a microelectronic mechanical structure (MEMS).

15. A method of making a MEMS device comprising:
   a forming a first sacrificial layer on a substrate;
   c. forming a MEM feature comprising an etch resistant material over the first sacrificial layer, the MEM structure layer having at least one gap therein;
   d. forming a second sacrificial layer on the MEM structure layer; and
   e. forming a capping layer over the second sacrificial layer.

16. The method of claim 15, further comprising:
   a. providing at least one access opening through the capping exposing a portion of the first sacrificial layer therebelow; and

   b. etching the first and the second sacrificial layers through the at least one access trench to release a portion of the MEM feature from the first and the

second sacrificial layers.

17. The method of claim 15, further comprising forming a bottom etch-stop layer on a process wafer prior to forming a first sacrificial layer.

18. The method of claim 16, wherein the etching is accomplished with an etchant comprising a noble gas fluoride.

19. The method of claim 16, wherein the etching is accomplished with an etchant comprising xenon difluoride.

20. A method of claim 16, further comprising sealing the at least one access opening with a sealing material.

21. A method of claim 20, wherein the sealing material is selected from the group consisting of metals, polymers and ceramics.

22. A structure for fabricating a MEMS comprising:
    a. a substrate;
    b. a capping layer over a portion of the substrate; and
    c. a release structure with release features, the release features being positioned between the wafer structure and embedded with a sacrificial material.

23. The structure of claim 22, wherein the sacrificial material is capable of being selectively etched relative to the capping layer by an etchant comprising a noble gas fluoride.

24. The structure of claim 22, wherein the etchant comprises Xenon Difluoride.

25. The structure of claim 22, wherein the sacrificial material is selectively etched relative to the capping layer by a rate (mass/time) of greater than 50:1.

26. The structure of claim 22, wherein the substrate comprises a layer of crystalline silicon.

27. The structure of claim 26, wherein the layer of crystalline silicon is doped with a dopant

28. The structure of claim 27, wherein the dopant comprises an element selected from the groups consisting of Boron and Phosphorus.

29. The structure of claim 22, wherein the substrate further comprises an etch-stop layer between the sacrificial material and the substrate.

30. The structure of claim 29, wherein the etch-stop layer comprising a material selected from the group consisting of oxides, oxynitrides and nitrites of silicon.

31. The structure of claim 22, wherein the capping layer comprises a plurality of access openings.

32. The structure of claim 22, wherein the sacrificial material comprises polysilicon.

33. The structure of claim 22, wherein the release structure comprises a material selected from the group consisting of oxides, oxynitrides and nitrites of silicon.

34. The structure of claim 22, wherein the capping layer comprises a material selected from the group consisting of oxides, oxynitrides and nitrites of silicon.

35. The structure of claim 22, wherein the release structure is a microelectronic mechanical structure (MEMS).

36. The structure of claim 22, further comprising an integrated circuit, wherein the integrated circuit is electrically couple to the release structure.

37. A structure for forming a plurality of interconnected cavities, comprising a multi-

layer structure comprising at least a first etch-stop layer, a second etch-stop layer, a capping layer, and polysilicon between the first and second etch-stop layers and between the second etch stop layer and the capping layer, the structure further comprising at least one internal passage in the second etch-stop layer for forming the plurality of interconnected cavities.

38. The structure of claim 37 further comprising at least hole through the capping for accessing the polysilicon thereunder.

39. The structure of claim 37, wherein the second etch-stop layer is patterned with release features and wherein the at least one internal passage is between the release features.

40. The structure of claim 39, wherein at least one of the release features is a portion of a MEMS oscillator.

41. The structure of claim 39, wherein a capping comprises and optical window that is transparent to one or more selected wavelengths of light.

42. A MEMS comprising:
    a. a wafer structure;
    b. a capping layer formed on the wafer structure; and
    c. a release structure comprising a plurality of movable release features encapsulated between the wafer structure and the capping layer.

43. The MEMS of claim 42, wherein the capping layer further comprises a plurality of sealed trenches.

44. The MEMS of claim 43, wherein the plurality of sealed trenches are sealed with a material selected from the group consisting of metals, polymers and ceramics

45. The MEMS of claim 44, wherein the plurality of sealed trenches are sealed with material comprising aluminum.

46. The MEMS of claim 42, wherein a portion the release structure comprises a layer of reflective material.

47. The MEMS of claim 46, wherein the reflective material comprises aluminum.

48. The MEMS of claim 42, wherein the capping layer comprises a material selected from the group consisting of oxides, oxynitrides and nitrites of silicon.

49. The MEMS of claim 48, wherein the capping layer has a thickness in a range of 1.0 to 3.0 microns.

50. The structure claim 42, wherein the release structure comprises a material selected from the group consisting of oxides, oxynitrides and nitrites of silicon.

51. The MEMS of claim 50, wherein the plurality of movable features have feature thickness in the range of 300 to 5000 Angstroms.

52. The MEMS of claim 42, further comprising an etch resistant layer between the wafer and the release structure.

53. The MEMS of claim 52, wherein the etch resistant layer comprises a material selected from the group consisting of oxides, oxynitrides and nitrites of silicon.

54. The MEMS of claim 53, wherein the etch resistant layer has a thickness in a range of 0.1 to 3.0 microns.

55. The MEMS of claim 42, further comprising an integrated circuit on the wafer structure, the integrated circuit being electrically coupled to the release structure.

56. The MEMS of claim 42, wherein the release structure comprises a resonator comb feature.

57. The MEMS of claim 42, wherein the release structure comprise a plurality of ribbon features.

58. The MEMS of claim 42, wherein the capping layer comprises at least one optical aperture for transmitting light through the capping layer.

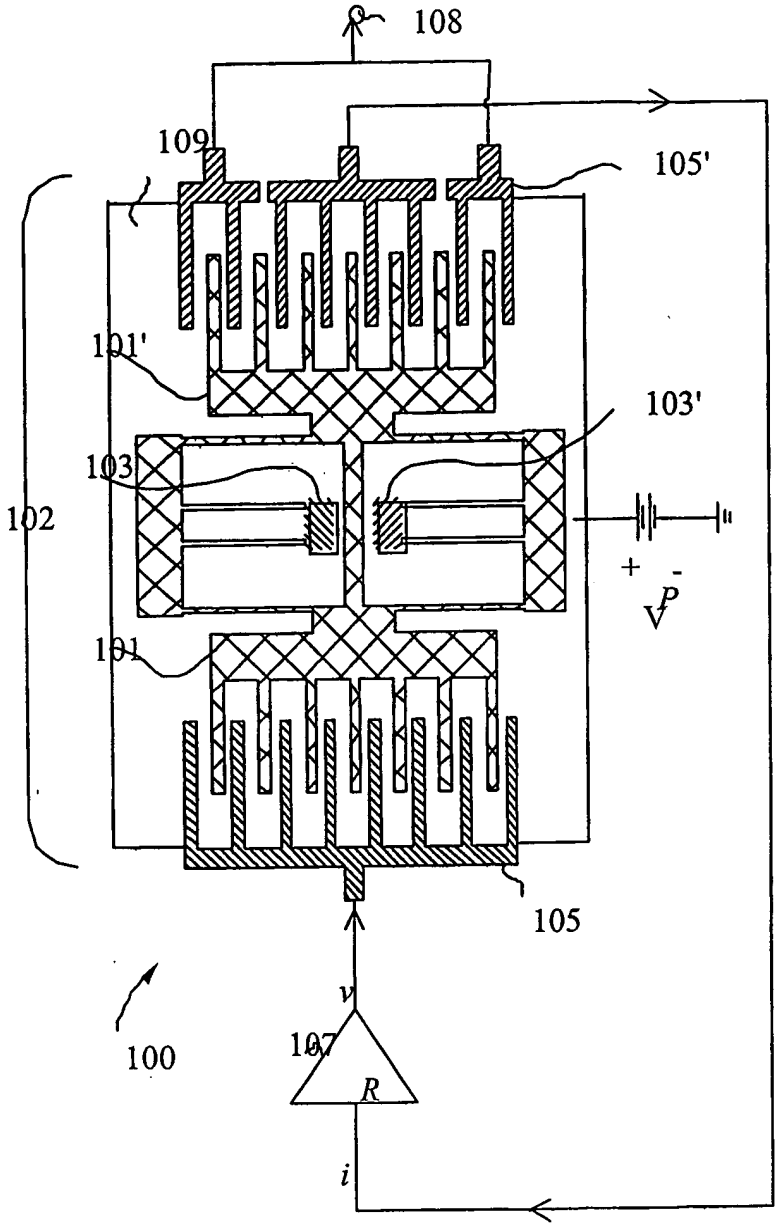


Fig. 1

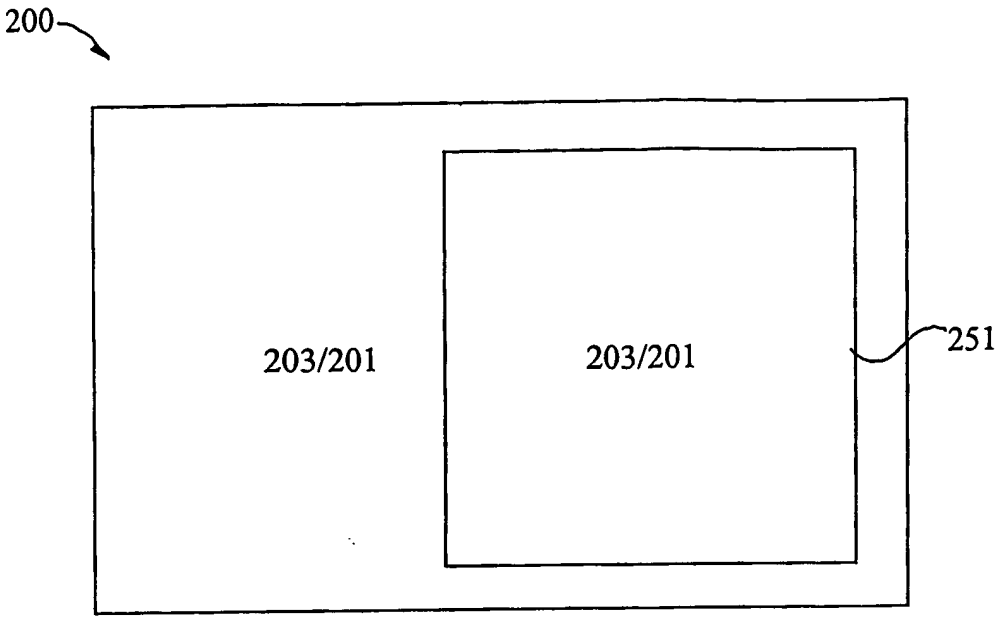


Fig. 2a

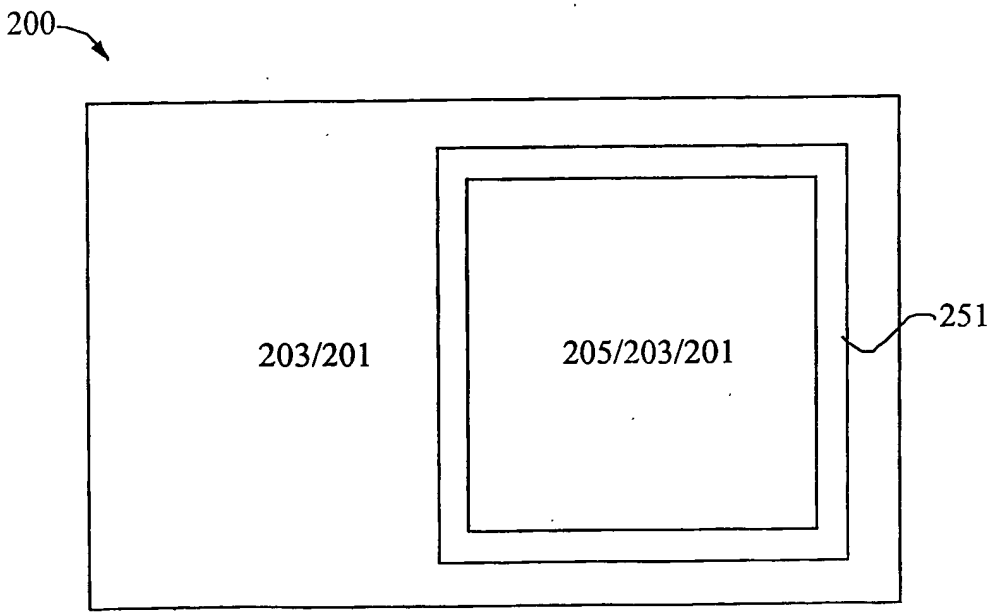
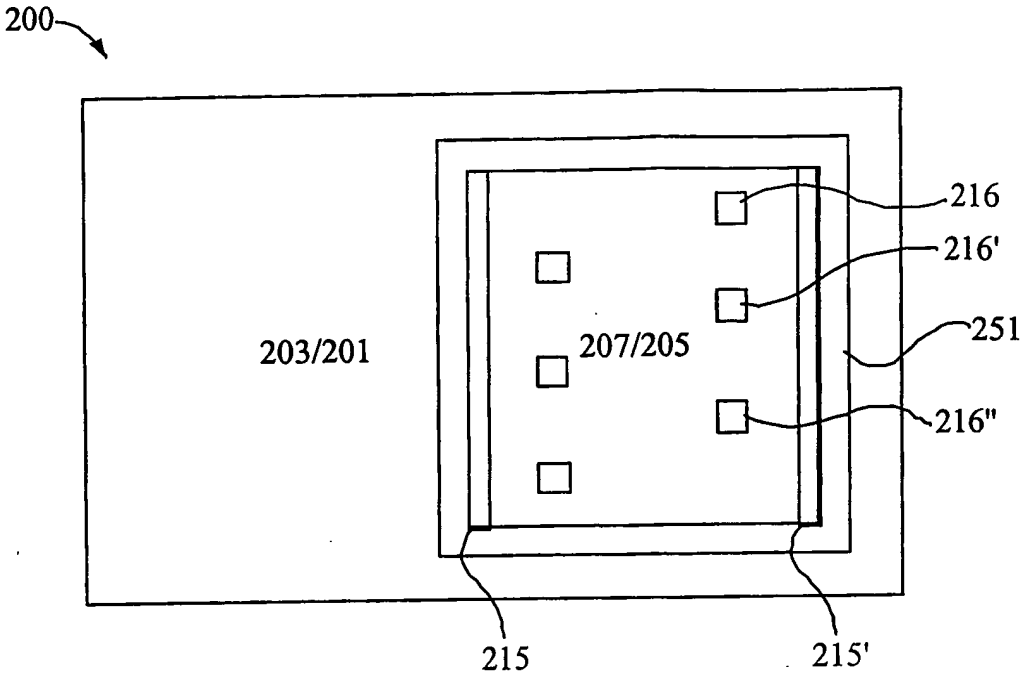


Fig. 2b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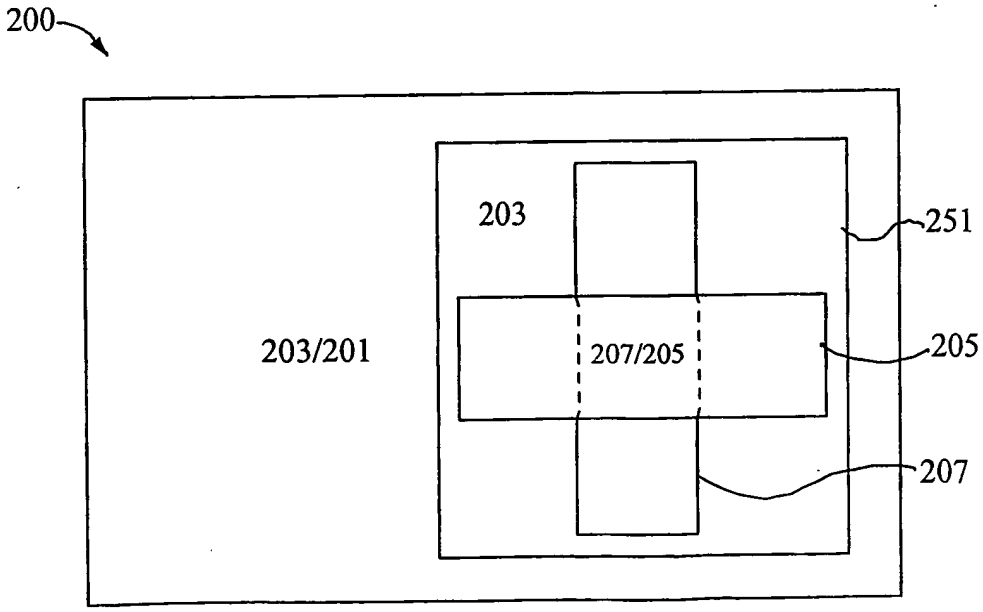
216
216'
251
203/201
207/205
216"
215
215'

Fig. 2c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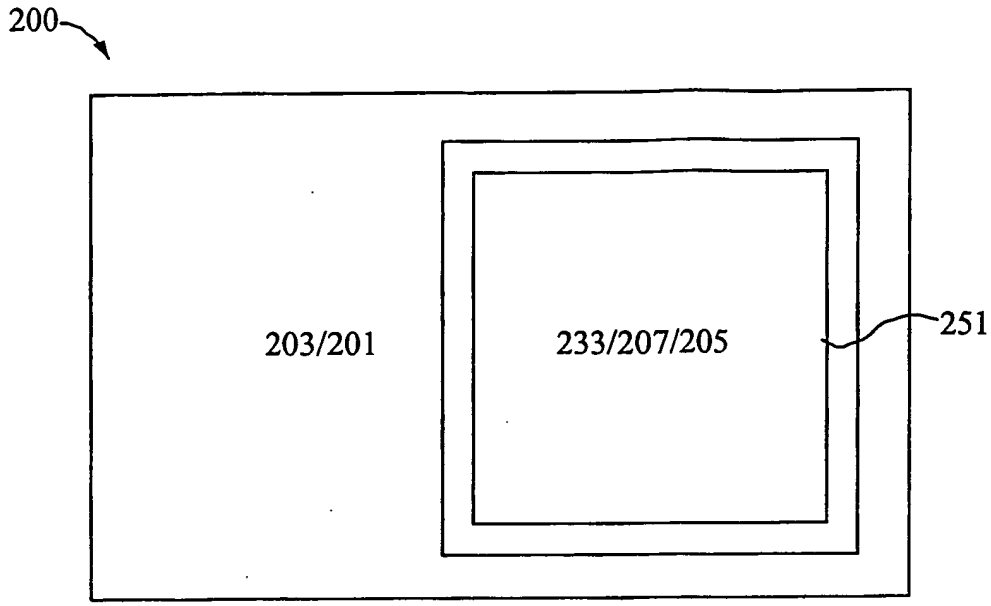
207/205
205
207

Fig. 2d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233/207/205
251

Fig. 2e

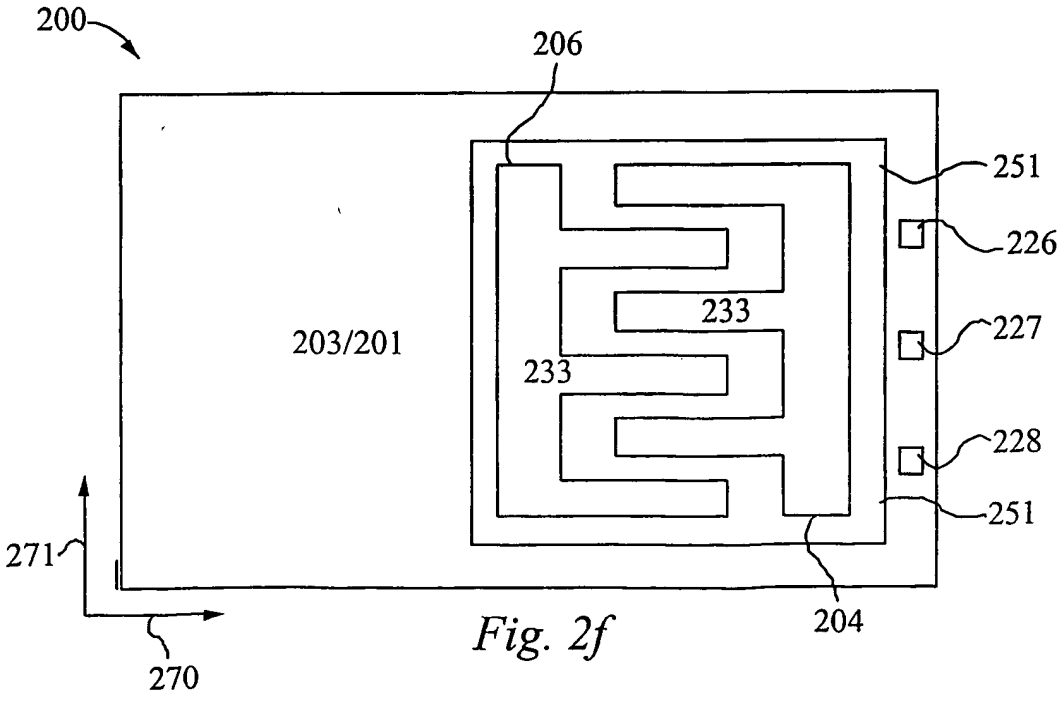
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Fig. 2f

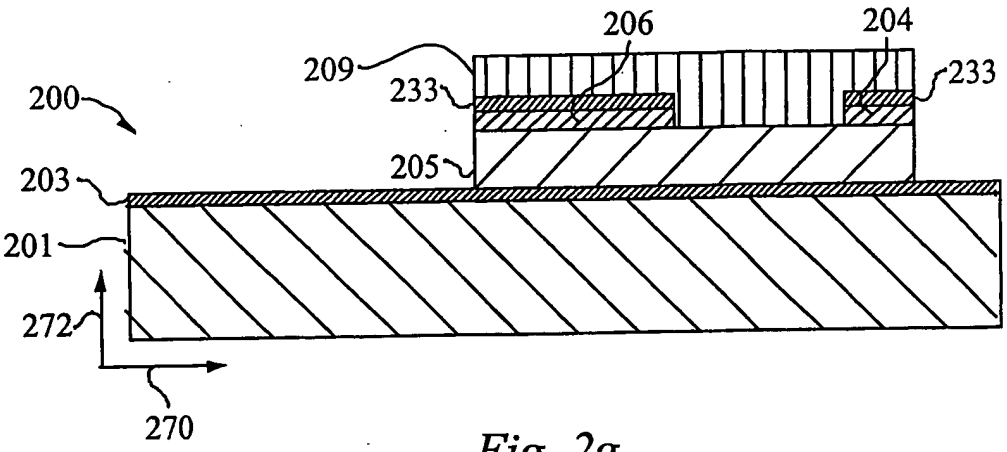
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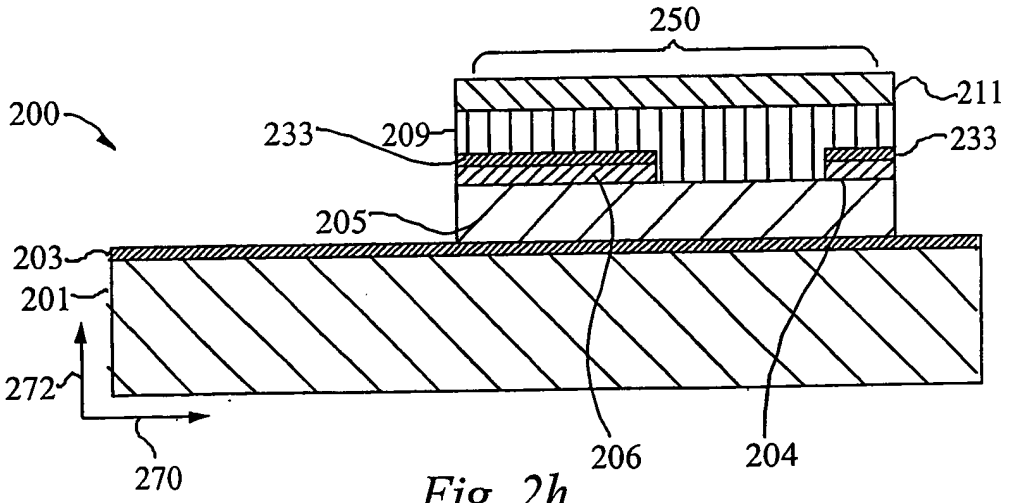
Fig. 2g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201
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270
206
204

Fig. 2h

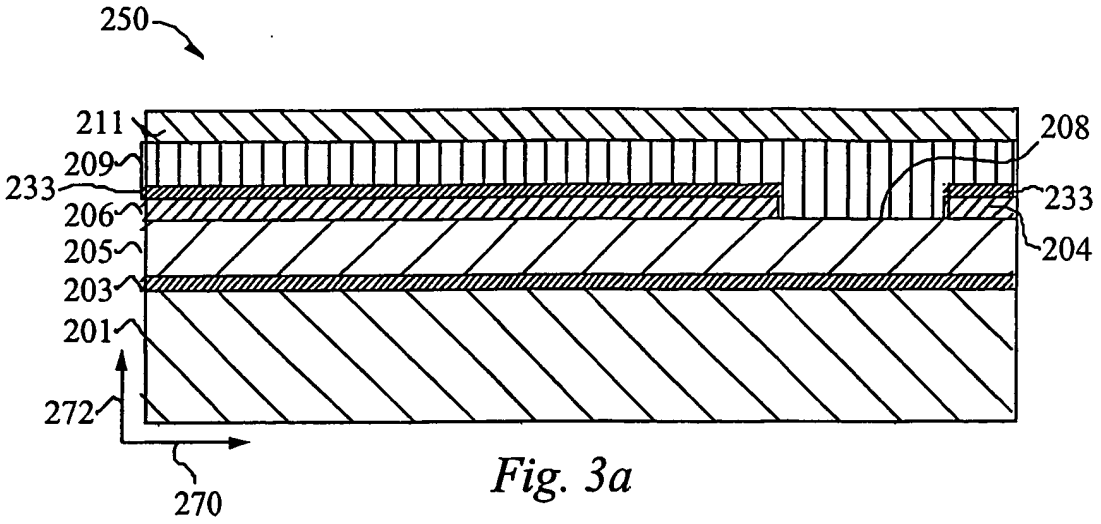

Fig. 3a

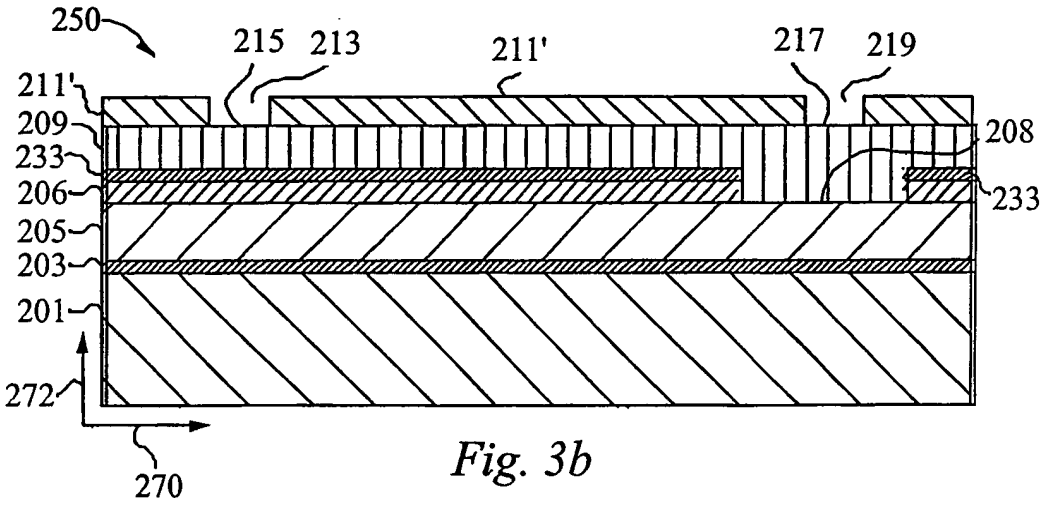

Fig. 3b

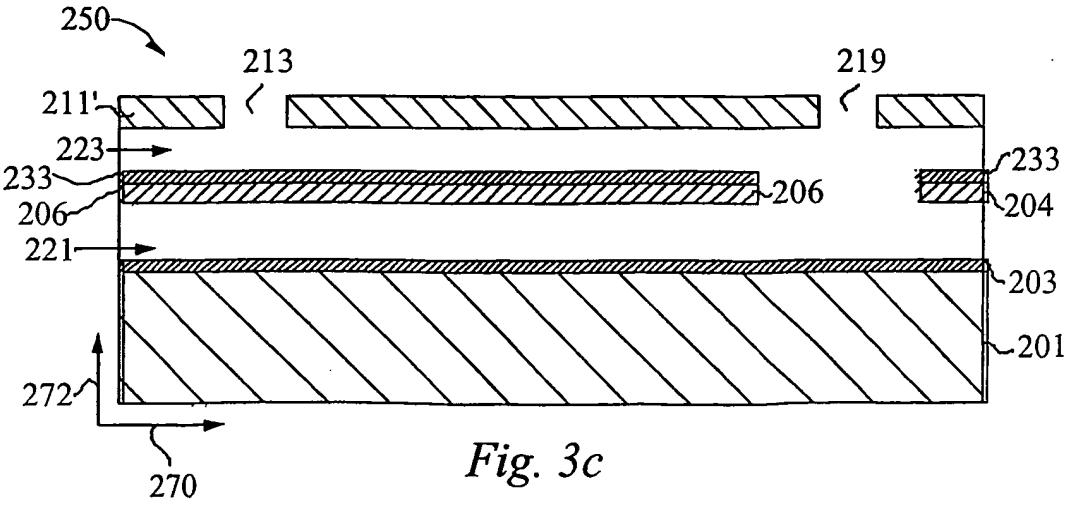

Fig. 3c

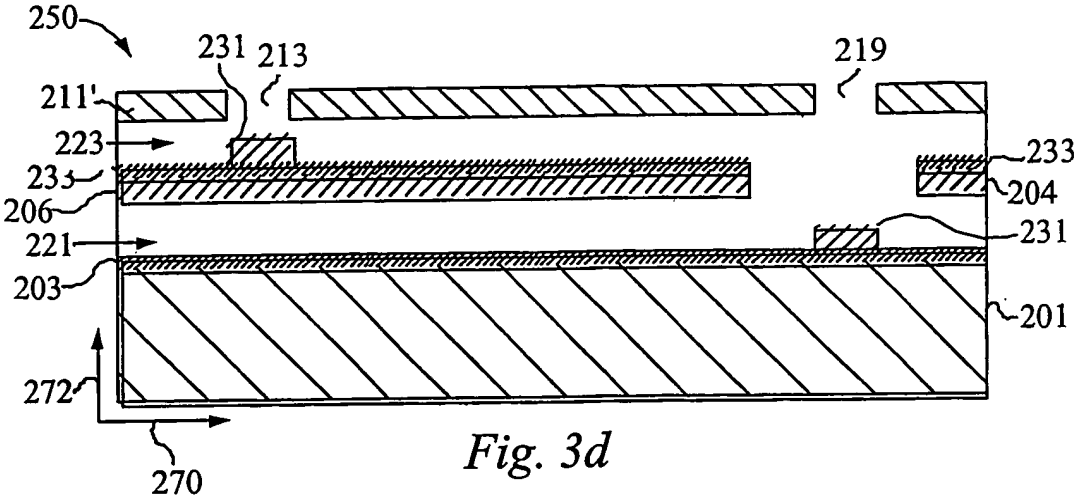

Fig. 3d

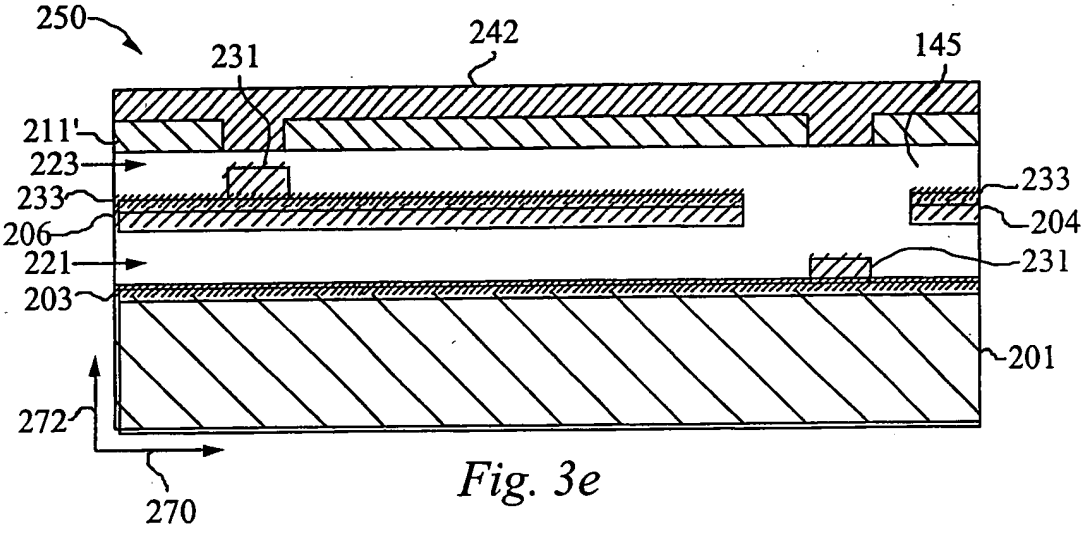

Fig. 3e

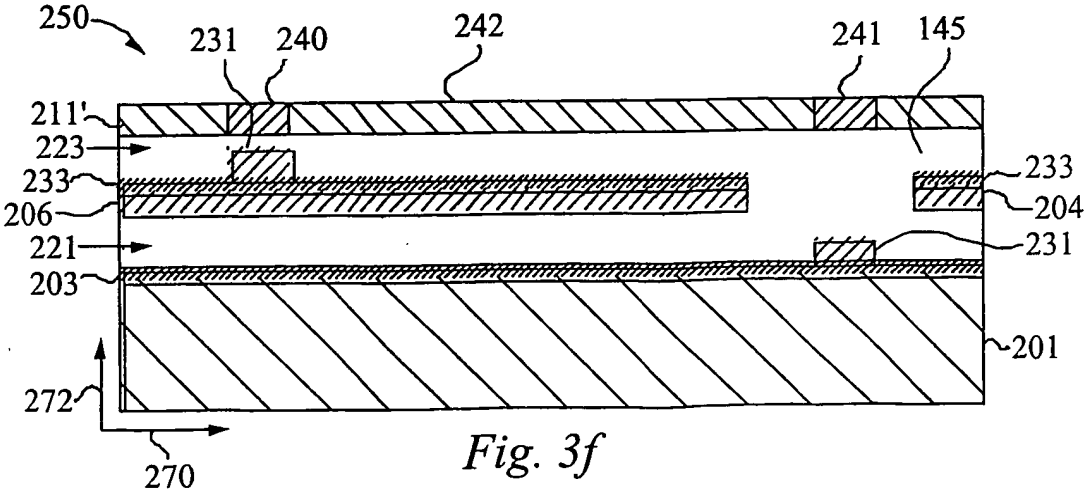

Fig. 3f

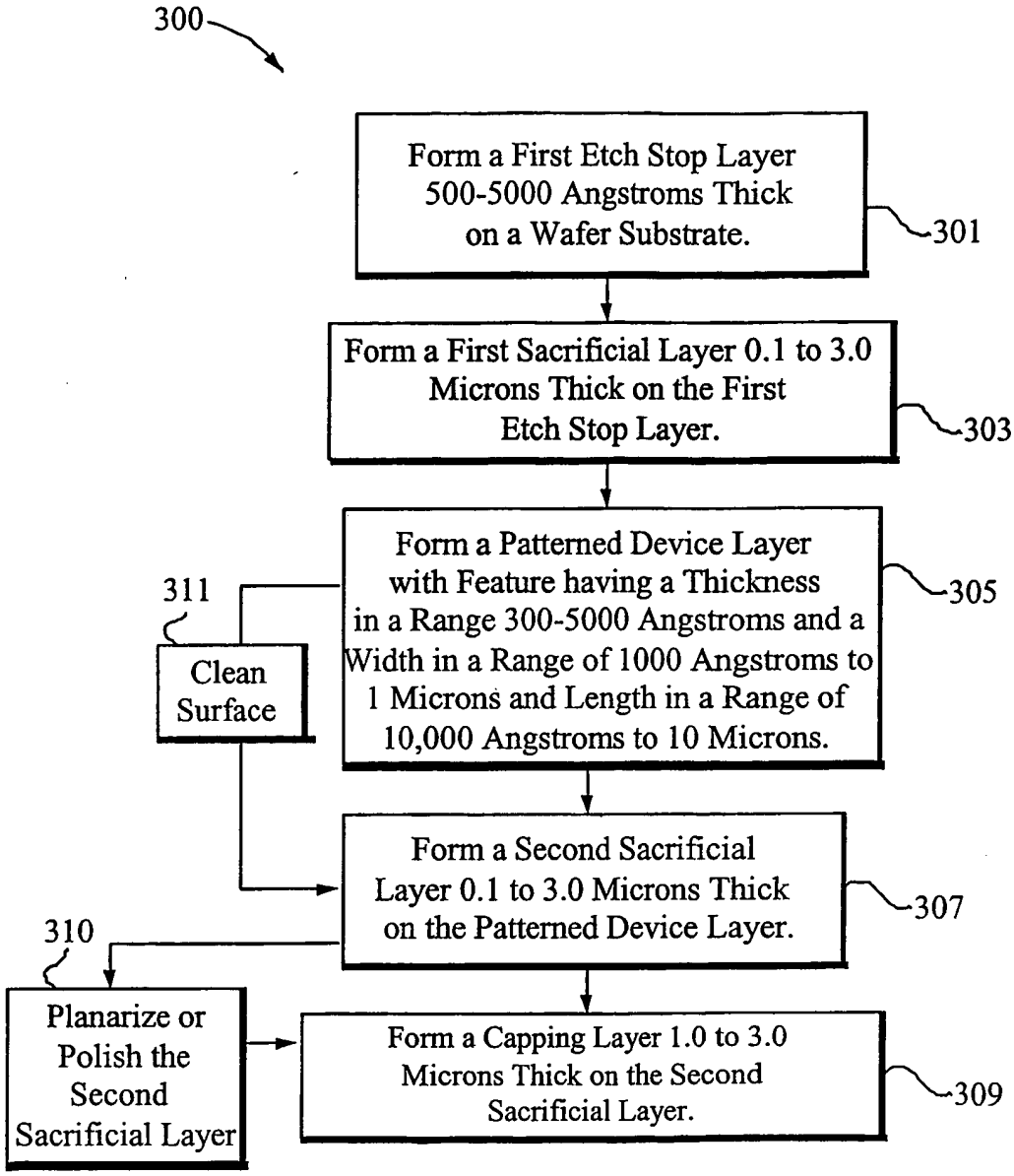
300
Form a First Etch Stop Layer 500-5000 Angstroms Thick on a Wafer Substrate.
301
Form a First Sacrificial Layer 0.1 to 3.0 Microns Thick on the First Etch Stop Layer.
303
Form a Patterned Device Layer with Feature having a Thickness in a Range 300-5000 Angstroms and a Width in a Range of 1000 Angstroms to 1 Microns and Length in a Range of 10,000 Angstroms to 10 Microns.
305
311
Clean Surface
Form a Second Sacrificial Layer 0.1 to 3.0 Microns Thick on the Patterned Device Layer.
307
310
Planarize or Polish the Second Sacrificial Layer
Form a Capping Layer 1.0 to 3.0 Microns Thick on the Second Sacrificial Layer.
309

Fig. 4

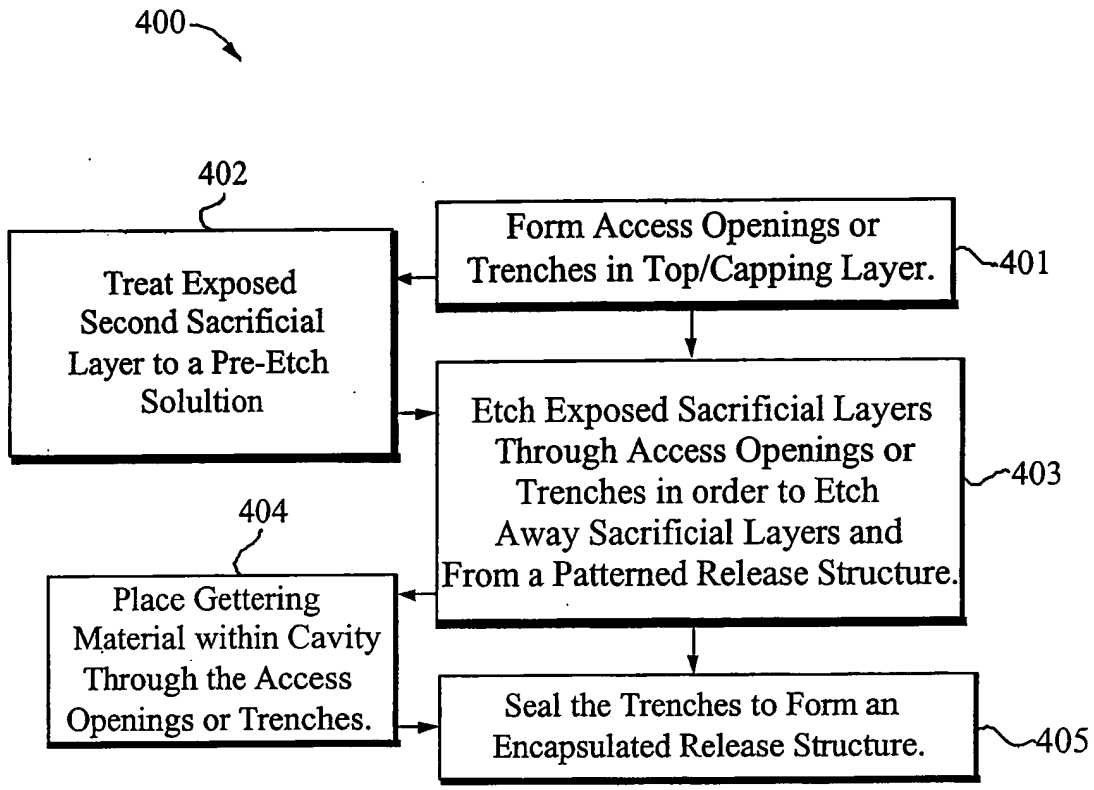
400
402
Treat Exposed Second Sacrificial Layer to a Pre-Etch Solultion
Form Access Openings or Trenches in Top/Capping Layer.
401
Etch Exposed Sacrificial Layers Through Access Openings or Trenches in order to Etch Away Sacrificial Layers and From a Patterned Release Structure.
403
404
Place Gettering Material within Cavity Through the Access Openings or Trenches.
Seal the Trenches to Form an Encapsulated Release Structure.
405

Fig. 5

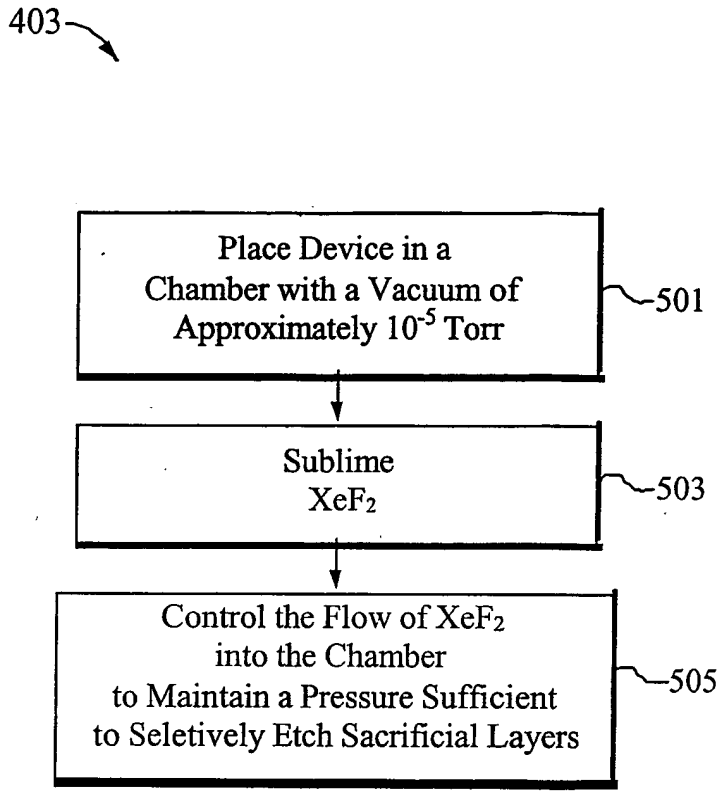
403
Place Device in a Chamber with a Vacuum of Approximately 10^{-5} Torr
501
Sublime XeF_2
503
Control the Flow of XeF_2 into the Chamber to Maintain a Pressure Sufficient to Seletively Etch Sacrificial Layers
505

Fig. 6

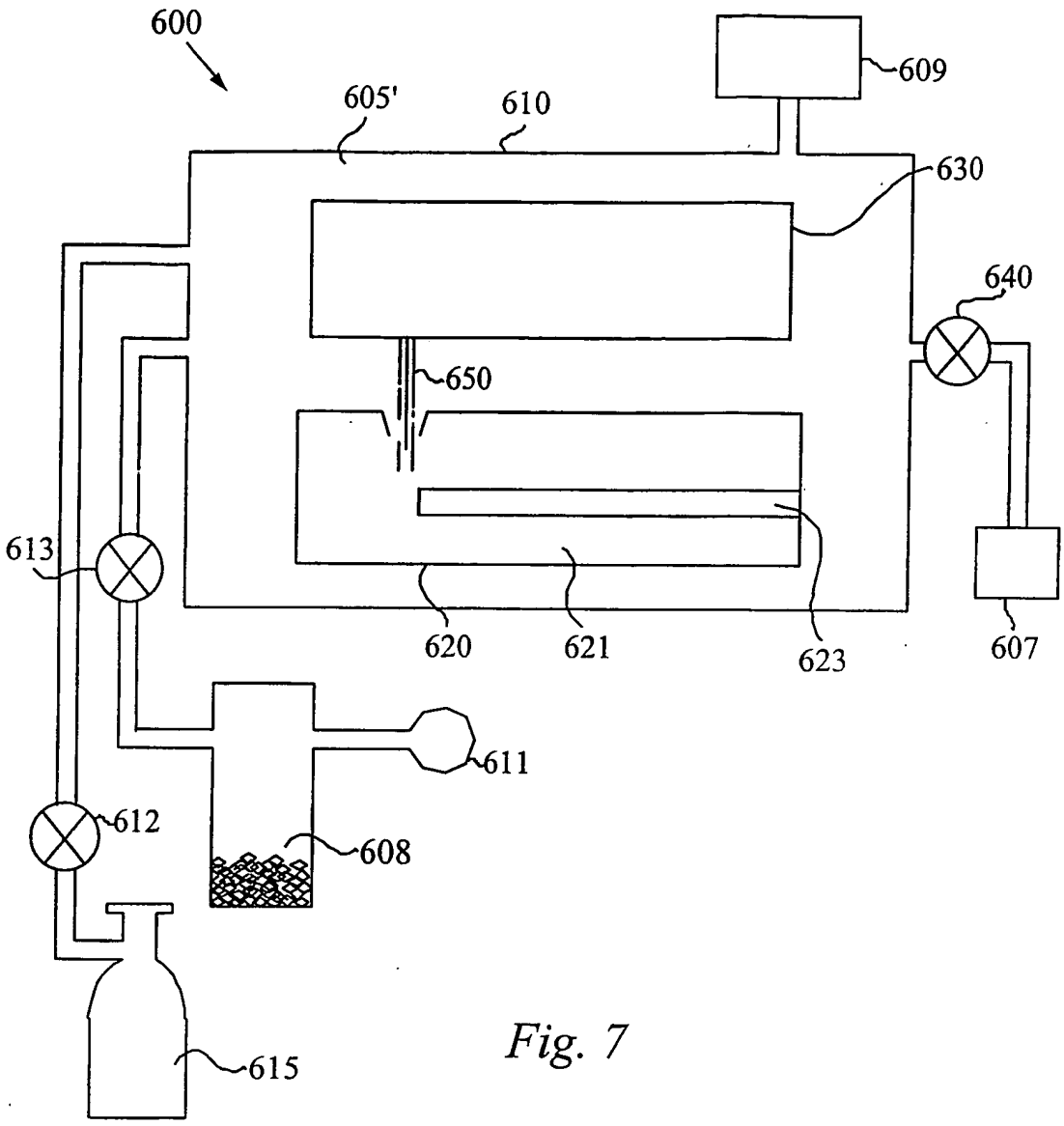

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/27822

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 23/02, 21/302, 21/461
US CL : 257/380; 438/735, 737, 738, 739, 740

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/380; 438/735, 737, 738, 739, 740; 216/2

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,919,548 A (Barron et al) 06 July 1999 (06.07.1999), column 6, line 59 to column 11, line 53.	1-36, 42-58
X	US 6,069,392 A (Tai et al) 30 May 2000 (30.05. 2000), column 4, line 7 to column 5, line 51.	1-58
X	US 6,123,985 A (Robinson et al) 26 September 2000 (26.09.2000), columns 3-6.	1-36, 42-58

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
01 November 2002 (01.11.2002)	08 NOV 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Amir Zarabian Telephone No. 703-3084905

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